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10/810,431	03/26/2004	Stephen Strickland	EMC04-02(04012)	9773

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EXAMINER	
SUGENT, JAMES F	
ART UNIT	**PAPER NUMBER**
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,431	STRICKLAND, STEPHEN	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,11-15 and 19-25* is/are rejected.

7)☒ Claim(s) *3,4,8-10 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received October 19, 2006 for application number 10/810,431 originally filed March 26, 2004. The Office hereby acknowledges receipt of the following and placed of record in file: claims 1-25 are presented for examination.

Information Disclosure Statement

The Information Disclosure Statement (IDS) submitted on July 24, 2006 was placed of record in file. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement is being considered by the Examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 6, 13, 14 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomlinson et al. (U.S. Patent No. 6,735,706 B2) (hereinafter referred to as Tomlinson) in view of Dougherty et al. (U.S. Patent No. 6,901,572 B1) (hereinafter referred to as Dougherty).

As to claim 1, Tomlinson discloses a data storage system, comprising: power circuitry configured to provide power signals (114 and 116); storage processing circuitry configured to perform data storage operations (processor coupled to 102 or 200 as shown in Figs. 1, 2 and 7; column 1, lines 11-25 and column 12, lines 24-35); and a packaged microcontroller (102 or 200) coupled to the power circuitry (as shown in Fig. 1) and the storage processing circuitry (as shown in Fig. 7), the packaged microcontroller having a set of input lines (at supervisor 112 or AIM[0-7] 204), a set of output lines (FET[0-3] within 207), and control circuitry (202) coupled to the set of input lines and the set of output lines (as shown in Fig. 2), the control circuitry being configured to: receive, on the set of input lines (at supervisor 112 or AIMs 204), a first set of power signals which is provided by the power circuitry to the storage processing circuitry (column 3, line 66 thru column 4, line 27 and column 4, line 54 thru column 5, line 20 and column 8, line 51 thru column 9, line 32), and output, through the set of output lines (FET[0-3] within 207), a set of enable signals to the power circuitry (via external FETs 128-134), the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry (column 4, lines 28-53 and column 5, lines 21-39).

Tomlinson fails to teach waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period.

Dougherty teaches a packaged power sequencing controller (50 or 55) to be used within a computing system (Fig. 3) comprising multivoltage devices (85) and power circuitry (input supply 3.3V in addition to 60, 65 and 80). The controller (55) comprising a set of inputs (90, 95 and 100) and a set of outputs (1.8V LDO enable, 2.5V Brick enable and 3.3V FET enable). Dougherty further teaches the controller waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period (column 3, lines 3-45 and column 10, lines 18-32). Dougherty has the additional feature of having the flexibility of programming the power controller in any manner desired by the programmer (column 1, lines 39-48 and column 2, lines 20-23).

It would have been obvious to one of ordinary skill of the art having the teachings of Tomlinson and Dougherty at the time the invention was made, to modify packaged microcontroller of Tomlinson to include the ability to wait a predetermined time period after the reception of an input signal before outputting an enable signal as taught by Dougherty. One of ordinary skill in the art would be motivated to make this combination of including the ability to wait a predetermined time period after the reception of an input signal before outputting an enable signal in view of the teachings of Dougherty, as doing so would give the added benefit of having the flexibility of programming the power controller in any manner desired by the programmer (as taught by Dougherty above).

As to claim 6, Tomlinson discloses a packaged microcontroller for controlling a data storage system having (i) power circuitry for providing power signals (114 and 116) and (ii) storage processing circuitry (processor) for performing data storage operations, the packaged microcontroller (102 or 200; column 1, lines 11-25 and column 12, lines 24-35) comprising: a set of input lines (at supervisor 112 or AIM[0-7] 204); a set of output lines (FET[0-3] within 207); and control circuitry (202) coupled to the set of input lines and the set of output lines (as shown in Figs. 2 and 7), the control circuitry being configured to: receive, on the set of input lines (at supervisor 112 or AIMs 204), a first set of power signals which is provided by the power circuitry to the storage processing circuitry (column 3, line 66 thru column 4, line 27 and column 4, line 54 thru column 5, line 20 and column 8, line 51 thru column 9, line 32), and output, through the set of output lines (FET[0-3] within 207), a set of enable signals to the power circuitry (via external FETs 128-134), the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry (column 4, lines 28-53 and column 5, lines 21-39).

Tomlinson fails to teach waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period.

Dougherty teaches a packaged power sequencing controller (50 or 55) to be used within a computing system (Fig. 3) comprising multivoltage devices (85) and power circuitry (input supply 3.3V in addition to 60, 65 and 80). The controller (55) comprising a set of inputs (90, 95 and 100) and a set of outputs (1.8V LDO enable, 2.5V Brick enable and 3.3V FET enable). Dougherty further teaches the controller waiting a predetermined time period in response to

receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period (column 3, lines 3-45 and column 10, lines 18-32). Dougherty has the additional feature of having the flexibility of programming the power controller in any manner desired by the programmer (column 1, lines 39-48 and column 2, lines 20-23).

It would have been obvious to one of ordinary skill of the art having the teachings of Tomlinson and Dougherty at the time the invention was made, to modify packaged microcontroller of Tomlinson to include the ability to wait a predetermined time period after the reception of an input signal before outputting an enable signal as taught by Dougherty. One of ordinary skill in the art would be motivated to make this combination of including the ability to wait a predetermined time period after the reception of an input signal before outputting an enable signal in view of the teachings of Dougherty, as doing so would give the added benefit of having the flexibility of programming the power controller in any manner desired by the programmer (as taught by Dougherty above).

As to claim 13, Tomlinson disclose a packaged microcontroller for controlling a data storage system having (i) power circuitry for providing power signals (114 and 116) and (ii) storage processing circuitry (processor) for performing data storage operations, the packaged microcontroller (102 or 200; column 1, lines 11-25 and column 12, lines 24-35) comprising: a set of input lines (at supervisor 112 or AIM[0-7] 204); a set of output lines (FET[0-3] within 207); and control circuitry (202) coupled to the set of input lines and the set of output lines (as shown in Figs. 2 and 7), the control circuitry including: means for receiving (at supervisor 112 or AIMs 204), on the set of input lines, a first set of power signals which is provided by the power

circuitry to the storage processing circuitry (column 3, line 66 thru column 4, line 27 and column 4, line 54 thru column 5, line 20 and column 8, line 51 thru column 9, line 32), and means for outputting (FET[0-3] within 207), through the set of output lines, a set of enable signals to the power circuitry (via external FETs 128-134), the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry (column 4, lines 28-53 and column 5, lines 21-39).

Tomlinson fails to teach waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period.

Dougherty teaches a packaged power sequencing controller (50 or 55) to be used within a computing system (Fig. 3) comprising multivoltage devices (85) and power circuitry (input supply 3.3V in addition to 60, 65 and 80). The controller (55) comprising a set of inputs (90, 95 and 100) and a set of outputs (1.8V LDO enable, 2.5V Brick enable and 3.3V FET enable). Dougherty further teaches the controller waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period (column 3, lines 3-45 and column 10, lines 18-32). Dougherty has the additional feature of having the flexibility of programming the power controller in any manner desired by the programmer (column 1, lines 39-48 and column 2, lines 20-23).

It would have been obvious to one of ordinary skill of the art having the teachings of Tomlinson and Dougherty at the time the invention was made, to modify packaged microcontroller of Tomlinson to include the ability to wait a predetermined time period after the

reception of an input signal before outputting an enable signal as taught by Dougherty. One of ordinary skill in the art would be motivated to make this combination of including the ability to wait a predetermined time period after the reception of an input signal before outputting an enable signal in view of the teachings of Dougherty, as doing so would give the added benefit of having the flexibility of programming the power controller in any manner desired by the programmer (as taught by Dougherty above).

As to claim 14, Tomlinson discloses in a packaged microcontroller, a method for controlling a data storage system having (i) power circuitry for providing power signals (114 and 116) and (ii) storage processing circuitry (processor) for performing data storage operations (column 1, lines 11-25 and column 12, lines 24-35), the method comprising: receiving (at supervisor 112 or AIMs 204), on a set of input lines of the packaged microcontroller (102 or 200), a first set of power signals which is provided by the power circuitry to the storage processing circuitry (column 3, line 66 thru column 4, line 27 and column 4, line 54 thru column 5, line 20 and column 8, line 51 thru column 9, line 32); and outputting (FET[0-3] within 207), on a set of output lines of the packaged microcontroller, a set of enable signals to the power circuitry, the set of enable signals directing the power circuitry to provide a second set of power signals to the storage processing circuitry (column 4, lines 28-53 and column 5, lines 21-39).

Tomlinson fails to teach waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period.

Dougherty teaches a packaged power sequencing controller (50 or 55) to be used within a computing system (Fig. 3) comprising multivoltage devices (85) and power circuitry (input

supply 3.3V in addition to 60, 65 and 80). The controller (55) comprising a set of inputs (90, 95 and 100) and a set of outputs (1.8V LDO enable, 2.5V Brick enable and 3.3V FET enable). Dougherty further teaches the controller waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines and outputting the enable signals after waiting the predetermined time period (column 3, lines 3-45 and column 10, lines 18-32). Dougherty has the additional feature of having the flexibility of programming the power controller in any manner desired by the programmer (column 1, lines 39-48 and column 2, lines 20-23).

It would have been obvious to one of ordinary skill of the art having the teachings of Tomlinson and Dougherty at the time the invention was made, to modify packaged microcontroller of Tomlinson to include the ability to wait a predetermined time period after the reception of an input signal before outputting an enable signal as taught by Dougherty. One of ordinary skill in the art would be motivated to make this combination of including the ability to wait a predetermined time period after the reception of an input signal before outputting an enable signal in view of the teachings of Dougherty, as doing so would give the added benefit of having the flexibility of programming the power controller in any manner desired by the programmer (as taught by Dougherty above).

As to claim 21, Tomlinson in combination with Dougherty taught the data storage system in claim 1, as shown above. Tomlinson further teaches the data storage system wherein the power circuitry includes a variety of power sources, each power source being configured to provide a power signal, which is at a distinct voltage from other power signals provided by other power sources, to an input line of a storage processing circuit of the storage processing circuitry

and to an input line of the packaged microcontroller which is separate from the input line of the storage processing circuit (column 1, line 66 thru column 2, line 16 and column 3, line 66 thru column 4, line 13).

As to claim 22, Tomlinson in combination with Dougherty taught the data storage system in claim 21, as shown above. Tomlinson further teaches the data storage system wherein the control circuitry is configured to: receive, on the set of input lines, a first set of power signals which is provided by the power circuitry to I/O buffer circuitry of the storage processing circuitry; and output, through the set of output lines, a set of enable signals to the power circuitry, the set of enable signals directing the power circuitry to provide a second set of power signals, the second set of power signals to power core circuitry of the storage processing circuitry (column 5, line 65 thru column 6, line 16).

Dougherty teaches further teaches waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines (column 3, lines 3-45).

As to claim 23, Tomlinson in combination with Dougherty taught the data storage system in claim 22, as shown above. Tomlinson further teaches the data storage system wherein the packaged microcontroller coupled to the power circuitry and the storage processing circuitry, the packaged microcontroller having a set of input lines, a set of output lines, and control circuitry coupled to the set of input lines and the set of output lines is a PIC-type microcontroller (column 4, line 54 thru column 5, line 39).

As to claim 24, Tomlinson in combination with Dougherty taught the packaged microcontroller in claim 6, as shown above. Tomlinson further teaches the packaged microcontroller wherein the control circuitry is configured to: receive, on the set of input lines, a

first set of power signals which is provided by the power circuitry to I/O buffer circuitry of the storage processing circuitry; and output, through the set of output lines, a set of enable signals to the power circuitry, the set of enable signals directing the power circuitry to provide a second set of power signals, the second set of power signals to power core circuitry of the storage processing circuitry (column 5, line 65 thru column 6, line 16).

Dougherty teaches further teaches waiting a predetermined time period in response to receipt of the first set of power signals on the set of input lines (column 3, lines 3-45).

As to claim 25, Tomlinson in combination with Dougherty taught the packaged microcontroller in claim 6, as shown above. Tomlinson further teaches the packaged microcontroller wherein the packaged microcontroller coupled to the power circuitry and the storage processing circuitry, the packaged microcontroller having a set of input lines, a set of output lines, and control circuitry coupled to the set of input lines and the set of output lines is a PIC-type microcontroller (column 4, line 54 thru column 5, line 39).

Claims 2, 5, 7, 11, 12, 15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomlinson in view of Dougherty as applied to claims 1, 6 and 14 above, and further in view of Orr et al. (U.S. Patent No. 6,850,048 B2) (hereinafter referred to as Orr).

As to claims 2, 7, and 15, both Tomlinson and Dougherty teach the power microcontroller and/or control circuitry being configured to compare values to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry. However, neither Tomlinson nor

Dougherty explicitly teach the packaged microcontroller further including a set of built-in analog-to-digital converters coupled to the set of input lines and to the control circuitry.

Orr teaches power supply microcontroller (10) that includes: a set of built-in analog-to-digital converters (48) coupled to the set of input lines and to the control circuitry (column 8, lines 55-65), the control circuitry (21 and 22 within 10) being configured to compare a set of binary values from the set of built-in analog-to-digital converters to a set of pre-determined thresholds to determine when all of the power signals within the set of power signals have reached levels that prevents damage to the storage processing circuitry when the second set of power signals is provided to the storage processing circuitry (Orr teaches input state machines 43 within the control circuits 21 and 22 receiving measured values that are received from A/D converters 48 and compared to a threshold; column 10, line 54 thru column 11, line 7). Orr has the additional feature of having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (column 2, lines 30-36).

It would have been obvious to one of ordinary skill of the art having the teachings of Amin, Brown and Orr at the time the invention was made, to modify microcontroller of Orr to include analog-to-digital converters and having the control circuitry of the microcontroller compares measured values to thresholds as taught by Orr. One of ordinary skill in the art would be motivated to make this combination of including analog-to-digital converters within the microcontroller and having the control circuitry of the microcontroller compares measured values to thresholds in view of the teachings of Orr, as doing so would give the added benefit of

having the ability to control a relatively arbitrary number of power supplies from various manufacturers with arbitrary voltage levels and varying sequences (as taught by Orr above).

As to claim 5, it is directed to the data storage system of steps set forth in claim 4. Therefore, it is rejected for the same basis as set forth hereinabove.

As to claims 11 and 12, they are directed to the packaged microcontroller of steps set forth in claim 7. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claims 19 and 20, they are directed to the method of steps set forth in claim 15. Therefore, they are rejected for the same basis as set forth hereinabove.

Allowable Subject Matter

Claims 3, 4, 8-10 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments, see page 14, line 18 thru page 15, line 14, filed October 19, 2006, with respect to the rejection(s) of claim(s) 1, 6, 13 and 14 under ***35 USC § 103*** have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tomlinson (as cited above) in combination with Dougherty (as cited above).

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
December 12, 2006

THUAN N. DU
PRIMARY EXAMINER